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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,486	07/29/2003	Koji Osafune	008312-0305258	5030
909	7590	09/09/2005	EXAMINER	
PILLSBURY WINTHROP SHAW PITTMAN, LLP			TZENG, FRED	
P.O. BOX 10500			ART UNIT	
MCLEAN, VA 22102			PAPER NUMBER	
			2651	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/628,486	Applicant(s) OSAFUNE, KOJI	
	Examiner Fred Tzeng	Art Unit 2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>7/29/03, 6/2/04, 5/17/05, 6/21/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.
3. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Claim 10 is objected to because of the following informalities: On page 34 line 21, "**reach** channel" should be replaced with "**read** channel" for claim 10 to be consistent with the instant application disclosure. Appropriate correction is required.

Art Unit: 2651

6. Claim 5 is objected to because of the following informalities: On page 32 line 17, "to performs" should be "to perform". Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 2, 7-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Genheimer et al (USPN 6,043,946), hereafter as Genheimer, in view of Ueno et al (USPN 5,918,001), hereafter as Ueno.

RE claim 1, Genheimer discloses the invention substantially as claimed. Genheimer discloses a disk drive (**see figure 1 and column 4 lines 25-27; i.e., the disk driver 10**) comprising: a head which reads data signals from any data region provided on a disk-shaped recording medium (**see figure 1 and column 4 lines 46-50; i.e., the head 28 read/write data on disk 18**); a phase-locked loop unit which generates a read clock signal (**see column 6 lines 41-46; i.e., the PLL generates clock signals for sampling/reading of the stored data**); a read channel which reproduces data from any data signal that the head has read from the disk-shaped recording medium (**see column 5 lines 65-67 and column 6 lines 1, 13-16; i.e., the read channel 70 which is the readback portion of the read/write channel 56 reproduces data from any data signal that the head 28 has read from the disc 18**);

Art Unit: 2651

in synchronism with the read clock signal generated by the phase-locked loop unit (**see column 6 lines 25, 27, 37-46; i.e., the self-synchronization between read channel 70 and the PLL**).

However, Genheimer does not specifically disclose a controller which alters a PLL parameter of the phase-locked loop unit when the data recorded by the read channel contains an error, the PLL parameter being related to a frequency-jitter part existing, due to the error, in PLL sync data recorded in the data region, and which performs a read-retry in accordance with the PLL parameter thus altered, to cause the read channel to read the data again.

Ueno teaches that if an error occurs while reading or writing data, the read/write manager 421 in the hard disk drive executes the error recovery by changing some standard reading conditions which includes altering the parameters of the PLL circuit to stabilize the sampling frequency, then to reread the data again (**see column 2 lines 1-16 and column 5 lines 27-35, 41-61**).

Genheimer and Ueno are combinable because they are from the same field of endeavor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Genheimer invention by including the read/write manager 421 from Ueno invention for executing an error recovery through altering a parameter of the PLL unit in order to enhance the system performance of a hard disk drive. Because by altering the parameters of the PLL circuit to stabilize the sampling frequency, less errors will occur while attempting to execute a retry to read the data again.

RE claim 2, Ueno in view of the rationale above discloses that the controller alters, as PLL parameter, any one of a plurality of operating parameters of the phase-locked loop unit, including a timing for acquisition mode, a gain for the acquisition mode and a gain for tracking mode (**see column 5 lines 57-59 and column 2 lines 9-10; i.e., the PLL gain adjustment and PLL center frequency adjustment teaches altering PLL parameters including a timing for acquisition mode and a gain for acquisition mode**).

RE claim 7, Genheimer in view of Ueno discloses the invention substantially claimed.

However, neither Genheimer nor Ueno discloses that the controller alters the PLL parameter of the phase-locked loop unit to set a gain for acquisition mode at a value lower than a value usually applied, and a gain for tracking mode at a value higher than a value usually applied.

But the uses of ranges are akin to optimizing the values of a result effective variable. Therefore, determining the optimal value of a result effective variable (i.e., the optimal gain value for the acquisition mode and tracking mode, respectively) would have been obvious and ordinary within the skill of the art. **In re Boesch**, 617 F.2d 272, 276, 205 USPQ 215, 219 (CCPA 1980).

RE claim 8, Genheimer discloses that the controller alters an operating parameter of the read channel, other than the PLL parameter, to perform an ordinary read-retry (**see column 3 lines 5-11**).

However, Genheimer does not disclose that alter any one of a plurality of operating parameters of the phase-locked loop unit to perform the read-retry when the ordinary read retry is unable to recover the error.

Ueno teaches alter any one of a plurality of operating parameters of the phase-locked loop unit to perform the read-retry when the ordinary read retry is unable to recover the error (**see column 2 lines 1-10**).

Genheimer and Ueno are combinable because they are from the same field of endeavor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Genheimer invention by including the read/write manager 421 from Ueno invention for executing an error recovery through altering a parameter of the PLL unit in order to enhance the system performance of a hard disk drive. Because by altering the parameters of the PLL circuit to stabilize the sampling frequency, less errors will occur while attempting to execute a retry to read the data again.

RE claim 9, Ueno in view of the rationale above discloses that the controller alters any one of the PLL parameters to perform the read-retry at first step, and alters an operating parameter of the read channel, other than the PLL parameter, to perform the ordinary read-retry again when the first step read-retry is unable to recover the error (**see column 5 lines 27-59**).

RE claim 10, Genheimer discloses the invention substantially as claimed. Genheimer discloses a disk drive (**see figure 1 and column 4 lines 25-27; i.e., the disk driver 10**) comprising: a head which reads data signals from any data region

Art Unit: 2651

provided on a disk-shaped recording medium (**see figure 1 and column 4 lines 46-50; i.e., the head 28 read/write data on disk 18**); a phase-locked loop unit which generates a read clock signal and which has a plurality of PLL parameters (**see column 6 lines 41-46; i.e., the PLL generates clock signals for sampling/reading of the stored data**); a read channel which reproduces data from any data signal that the head has read from the disk-shaped recording medium (**see column 5 lines 65-67 and column 6 lines 1, 13-16; i.e., the read channel 70 which is the readback portion of the read/write channel 56 reproduces data from any data signal that the head 28 has read from the disc 18**); in synchronism with the read clock signal generated by the phase-locked loop unit (**see column 6 lines 25, 27, 37-46; i.e., the self-synchronization between read channel 70 and the PLL**); a detecting unit which detects an operating condition of the phase-locked loop unit (**see column 7 lines 46-49; i.e., detecting the operating condition of the PLL circuit by adjusting its operating frequency**).

However, Genheimer does not specifically disclose a PLL control unit which alters any one of the PLL parameters of the phase-locked loop unit, including a timing for acquisition mode, a gain for the acquisition mode and a gain for tracking mode as well as a controller which alters any one of the PLL parameters when the detecting unit detects that the phase-locked loop unit is operating in an abnormal condition due to an error in the data reproduced by the read channel, and which cause the read channel to read the data again in accordance with the PLL parameter altered.

Ueno teaches that if an error occurs while reading or writing data, the read/write manager 421 in the hard disk drive executes the error recovery by changing some standard reading conditions which includes altering the parameters of the PLL circuit to stabilize the sampling frequency, then to reread the data again (**see column 2 lines 1-16 and column 5 lines 27-35, 41-61**).

Genheimer and Ueno are combinable because they are from the same field of endeavor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Genheimer invention by including the read/write manager 421 from Ueno invention for executing an error recovery through altering a parameter of the PLL unit in order to enhance the system performance of a hard disk drive. Because by altering the parameters of the PLL circuit to stabilize the sampling frequency, less errors will occur while attempting to execute a retry to read the data again.

RE claim 11, Genheimer in view of rationale above discloses that the controller causes the read channel to perform an ordinary read-retry in accordance with an operation parameter of the read channel, other than the plurality of PLL parameters, when the phase-locked loop unit operates in a normal condition (**see column 3 lines 5-11**).

RE claim 12, Ueno in view of the rationale above discloses that the detecting unit acquires, as data representing the operating condition of the phase-locked loop unit, information about a phase error or a frequency error made in acquisition mode or in tracking mode (**see column 5 lines 27-59; i.e., the read/write manager 421**

functioned as the detecting unit acquires information about a phase error or frequency error made in acquisition mode or in tracking mode through PLL center frequency adjustment).

RE claim 13, Ueno in view of the rationale above discloses that the controller causes the read channel to perform a read-retry in accordance with information obtained from the detecting unit when the phase error or frequency error made in the acquisition mode or in the tracking mode exceeds a permissible value **(see column 5 lines 48-51; i.e., a read-retry is performed after error recovery subroutine being executed sequentially in the ERP if error exceeds permissible value).**

RE claim 14, Genheimer discloses the invention substantially as claimed. Genheimer discloses a disk drive **(see figure 1 and column 4 lines 25-27; i.e., the disk driver 10)** comprising: a head which reads data signals from any data region provided on a disk-shaped recording medium **(see figure 1 and column 4 lines 46-50; i.e., the head 28 read/write data on disk 18)**; a read channel which reproduces data from any data signal that the head has read **(see column 5 lines 65-67 and column 6 lines 1, 13-16; i.e., the read channel 70 which is the readback portion of the read/write channel 56 reproduces data from any data signal that the head 28 has read from the disc 18).**

However, Genheimer does not specifically disclose a controller which causes the read channel to perform a read-retry when an error occurs in data reproduced by the read channel and cause the head to write, in the data region, the same data that the head has read, when the error is recovery by the read-retry.

Ueno teaches that if an error occurs while reading or writing data, the read/write manager 421 in the hard disk drive executes the error recovery by changing some standard reading conditions which includes altering the parameters of the PLL circuit to stabilize the sampling frequency, then to reread or write the data again **(see column 2 lines 1-16 and column 5 lines 27-35, 41-61)**.

Genheimer and Ueno are combinable because they are from the same field of endeavor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Genheimer invention by including the read/write manager 421 from Ueno invention for executing an error recovery through altering a parameter of the PLL unit in order to enhance the system performance of a hard disk drive. Because by altering the parameters of the PLL circuit to stabilize the sampling frequency, less errors will occur while attempting to execute a retry to read the data or write the same data that the head has read again.

RE claim 15, Ueno in view of the rationale above discloses a verification unit which reads and verifies data after the head has written the data under control of the controller **(see column 5 lines 27-35; i.e., the ERP verifies data by verifying if read errors has been recovery)**.

RE claim 16, Ueno in view of the rationale above discloses that an unit which causes the head to write the data in a data region other than the data region from which the read channel has read the data, when the verification unit detects an error in the data **(see column 5 lines 35-40; i.e., the data reassignment is executed to cause the head to write the data in a spare data region other than the data region from**

Art Unit: 2651

which the read channel has read the data, when the verification unit detects an error in the data).

RE claim 17, Genheimer discloses the invention substantially as claimed.

Genheimer discloses a read channel for reproducing data from a disk medium by using a head in a disk drive **(see column 5 lines 65-67 and column 6 lines 1, 13-16; i.e., the read channel 70 which is the readback portion of the read/write channel 56 reproduces data from any data signal that the head 28 has read from the disc 18 in disk drive 10)**, comprising: a phase-locked loop unit which has a plurality of PLL parameters **(see column 7 lines 46-49; i.e., the gain or the frequency parameters of the PLL unit)** and which generates a read clock signal required in reproducing data from the disk medium **(see column 6 lines 41-46; i.e., the PLL unit generates clock signals for sampling/reading of the stored data).**

However, Genheimer does not specifically disclose a PLL control unit which sets or alters any one of the PLL parameters including a timing for acquisition mode, a gain for the acquisition mode and a gain for tracking mode and a unit which transmits information about an operating condition of the phase-locked loop unit, to an external device, the information representing a phase error or frequency error made in the acquisition mode or in the tracking mode.

Ueno teaches that if an error occurs while reading or writing data, the read/write manager 421 in the hard disk drive executes the error recovery by changing some standard reading conditions which includes altering the parameters of the PLL circuit to stabilize the sampling frequency, then to reread the data again **(see column 2 lines 1-**

Art Unit: 2651

16 and column 5 lines 27-35, 41-61), wherein the PLL parameters including a timing for acquisition mode, a gain for the acquisition mode and a gain for tracking mode (see column 5 lines 51-59 and column 1 lines 1-10).

Genheimer and Ueno are combinable because they are from the same field of endeavor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Genheimer invention by including the read/write manager 421 from Ueno invention for executing an error recovery through altering a parameter of the PLL unit in order to enhance the system performance of a hard disk drive. Because by altering the parameters of the PLL circuit to stabilize the sampling frequency, less errors will occur while attempting to execute a retry to read the data again.

RE claim 18, Genheimer discloses the invention substantially as claimed. Genheimer discloses a method of reproducing data from a disk medium by using a head in synchronism with a read clock signal generated by a phase-locked loop unit in a disk drive **(see column 5 lines 65-67 and column 6 lines 1, 13-16; i.e., the read channel 70 which is the readback portion of the read/write channel 56 reproduces data from any data signal that the head 28 has read from the disc 18 in disk drive 10)**, the method comprising: performing an ordinary read-retry when a read error is made while the head is reproducing the data from the disk medium **(see column 2 lines 36-41).**

However, Genheimer does not specifically disclose performing a read-retry when the ordinary read-retry fails to recover the read error, by altering any one of PLL

Art Unit: 2651

parameters of the phase-locked loop unit, including a timing for acquisition mode, a gain for the acquisition mode and a gain for tracking mode.

Ueno teaches that if an error occurs while reading or writing data, the read/write manager 421 in the hard disk drive executes the error recovery by changing some standard reading conditions which includes altering the parameters of the PLL circuit to stabilize the sampling frequency, then to reread the data again (**see column 2 lines 1-16 and column 5 lines 27-35, 41-61**), wherein the PLL parameters including a timing for acquisition mode, a gain for the acquisition mode and a gain for tracking mode (**see column 5 lines 51-59 and column 1 lines 1-10**).

Genheimer and Ueno are combinable because they are from the same field of endeavor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Genheimer invention by including the read/write manager 421 from Ueno invention for executing an error recovery through altering a parameter of the PLL unit in order to enhance the system performance of a hard disk drive. Because by altering the parameters of the PLL circuit to stabilize the sampling frequency, less errors will occur while attempting to execute a retry to read the data again.

RE claim 19, Ueno in view of the rationale above discloses that detecting an operating condition of the phase-locked loop unit when a read error is made while the head is reproducing the data from the disk medium (**see column 5 lines 27-59; i.e., the read/write manager 421 functioned as the detecting unit acquires information about a phase error or frequency error made in acquisition mode or in tracking**

Art Unit: 2651

mode through PLL center frequency adjustment); and performing a read-retry by altering any one of the PLL parameters, when the operating condition of the phase-locked loop unit exceeds a permissible value (see column 5 lines 48-51; i.e., a read-retry is performed after error recovery subroutine being executed sequentially in the ERP if error exceeds permissible value).

RE claim 20, Ueno in view of the rationale above discloses that writing data in a data region of the disk medium when the read-retry recovers the error, the data being the same data the head has read from the data region (see column 5 lines 27-35; i.e., if the read-retry recovers the error, control is returned to the read/write manager 421 for data reading or writing which including writing the same data the head has read).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Genheimer et al (USPN 6,043,946), hereafter as Genheimer, in view of Ueno et al (USPN 5,918,001), hereafter as Ueno, and further in view of Sutardja (USPN 6,732,286).

RE claims 3 and 4, Genheimer in view of Ueno disclose the invention substantially as claimed.

However, neither Genheimer nor Ueno discloses that the controller alters a timing for acquisition mode and a gain for the acquisition mode at a value lower than a value usually applied, selected from a plurality of operating parameters of the phase-locked loop unit, and alters a combination of the parameters, as PLL parameter, to perform the read-retry.

Sutardja teaches an invention to use type I circuit while in the acquisition mode and simultaneously calculating an estimated value of frequency offset, such that the timing frequency can be adjusted prior to existing acquisition mode and entering tracking mode (**see column 5 lines 60-65**) as well as reducing the bandwidth to a low value so that the type II circuit can operate in tracking mode while maintaining stability of the timing circuit (**see column 5 lines 66-67 and column 6 lines 1-8**) for a data recovery system, which may be referred to as a channel, invariably requires a timing recovery feedback loop for clock synchronization through the use of a phase-locked loop which typically operating in an acquisition mode and an tracking mode (**see column 1 lines 13-32**).

Genheimer, Ueno and Sutardja are combinable because they are from the same field of endeavor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Genheimer and Ueno inventions by including the invention for altering a timing for acquisition mode and a gain for the acquisition mode and its combination by calculating an estimated value of frequency

offset using type I and II circuits from Sutardja in order to provide a high speed read channel while reducing high latency for data recovery as expressly stated at column 1 lines 10-15 of Sutardja.

RE claims 5 and 6, Genheimer in view of Ueno disclose the invention substantially as claimed.

However, neither Genheimer nor Ueno discloses that the controller has means of altering, as PLL parameter, any one of a plurality of operating parameters of the phase-locked loop unit, including a timing for acquisition mode, a gain for the acquisition mode and a gain for tracking mode; alters a combination of the timing and the gain, both for acquisition mode, as PLL parameter, to perform the read-retry; and changes the timing and gain for acquisition mode, back to normal values and alters the gain for tracking mode to perform the read retry, when the read retry is unable to recover the error.

Sutardja teaches an invention to use type I circuit while in the acquisition mode and simultaneously calculating an estimated value of frequency offset, such that the timing frequency can be adjusted prior to existing acquisition mode and entering tracking mode (**see column 5 lines 60-65**) as well as reducing the bandwidth to a low value so that the type II circuit can operate in tracking mode while maintaining stability of the timing circuit (**see column 5 lines 66-67 and column 6 lines 1-8**) for a data recovery system, which may be referred to as a channel, invariably requires a timing recovery feedback loop for clock synchronization through the use of a phase-locked loop which typically operating in an acquisition mode and an tracking mode (**see column 1 lines 13-32**).

Genheimer, Ueno and Sutardja are combinable because they are from the same field of endeavor. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Genheimer and Ueno inventions by including the invention for altering a timing for acquisition mode and a gain for the acquisition mode and its combination by calculating an estimated value of frequency offset using type I and II circuits from Sutardja in order to provide a high speed read channel while reducing high latency for data recovery as expressly stated at column 1 lines 10-15 of Sutardja.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

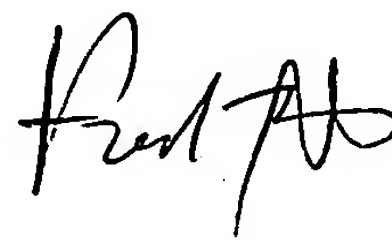
12. Any inquiry concerning this communication from the examiner should be directed to Fred Tzeng whose telephone number is 571-272-7565. The examiner can normally be reached on weekdays from 9:30 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on 571-272-7843. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8400 for regular communications and 571-273-7565 for After Final communications.

13. Informal regarding the status of an application may be obtained from the Patent Application Information Retrieval (**PAIR**) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

Art Unit: 2651

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read "Fred F. Tzeng". The signature is stylized with a large, looped "F" and a cursive "Tzeng".

Fred F. Tzeng

September 2, 2005